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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte KULJIT BAINS

Appeal 2019-003979
Application 13/531,368[1]
Technology Center 2100

Before MARC S. HOFF, JASON J. CHUNG and JOHN D. HAMANN, *Administrative Patent Judges*.

HOFF, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF THE CASE

Appellant appeals under 35 U.S.C. § 134 from a Final Rejection of claims 1, 4-8, 10-14, 16, 18-22, 24, 26-29, 31, 32, 34-42, 44-48, and 52-54.[2] We have jurisdiction under 35 U.S.C. § 6(b).

We reverse.

Appellant's invention concerns programming an operation mode of a dynamic access memory (DRAM) device. A memory controller stores a value in a mode register, specifying whether a per-DRAM addressability

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[1] Appellant states that the real party in interest is Intel Corporation. Appeal Br. 2.

[2] Claims 2, 3, 9, 15, 17, 23, 25, 30, 33, 43, and 49–51 have been cancelled.

(PDA) mode of the DRAM device is enabled. An external contact of the DRAM device is coupled to the memory controller device via a signal line of a data bus. Abstract. In an embodiment, a DRAM device may require write leveling before entering PDA mode. Spec. ¶ 16.

Claim 1 is reproduced below:

1. A dynamic random access memory (DRAM) device comprising:
a memory array;
an external contact to couple the DRAM device to a signal line DQ0 of a data bus;
a mode register to store a value to indicate whether a per-DRAM addressability (PDA) mode of the DRAM device is enabled, the PDA mode to indicate that only selected DRAMs of a rank of multiple DRAMs are to process a command to make changes to a configuration setting, wherein the rank of multiple DRAMs includes the multiple DRAMs in parallel which all execute memory access commands in parallel when PDA mode is not enabled, wherein as a condition to a change of the value to enable the PDA mode the DRAM device is to perform write leveling; and
control logic coupled to the mode register, wherein, while the PDA mode of the DRAM device is enabled, the control logic is to condition programmability of one or more features of the DRAM device upon detection of a signal received via DQ0, including to select between execution of a received command and forego execution of the received command based on a logic value of the signal received via DQ0, wherein the control logic is to sample DQ0 during a sequence of a burst of data strobe signals to determine the logic value, wherein the sample is to be after a first rising edge of the burst of data strobe signals, on either a first falling edge or on a second rising edge of the burst of data strobe signals.

The prior art relied upon by the Examiner as evidence is:

Name	Reference	Date
MacWilliams	US 2007/0013704 A1	Jan. 18, 2007
Jeon	US 2011/0047319 A1	Feb. 24, 2011
Cordero	US 2013/0339821 A1	Dec. 19, 2013
JEDEC1	SDRAM Standard JESD79-3F	Jul. 2010
JEDEC2	JEDEC Mini Workshop, Server Memory Forum	2011
Kinsley	DDR4 "Module Level Trends and Features" Micron Technology, Server Memory Forum	2011
JEDEC3	Migrating to LPDDR3, LPDDR3 Symposium	2012
Keller	JEDEC Server Memory Forum: Shenzhen Agenda	2015

Claims 1, 4-8, 10-14, 16, 18-22, 24, 26-29, 31, 32, 34-37, 39-42, 44-48, and 52-54 stand rejected under 35 U.S.C. § 112(a) or 35 U.S.C. § 112 (pre-AIA), first paragraph, as failing to comply with the written description requirement. Final Act. 3.

Claims 1, 8, 14, 16, 22, 24, and 29 stand rejected under 35 U.S.C. § 103 as being unpatentable over Kinsley, Cordero, MacWilliams, and Jeon. Final Act. 4.

Claims 31, 36, 40, 41, 44, and 52-54 stand rejected under 35 U.S.C. § 103 as being unpatentable over Kinsley, Cordero, MacWilliams, Jeon, and JEDEC1. Final Act. 9.

Claims 6, 10, 18, and 26 stand rejected under 35 U.S.C. § 103 as being unpatentable over Kinsley, Cordero, MacWilliams, Jeon,[3] and JEDEC1. Final Act. 11.

Claims 45-48 stand rejected under 35 U.S.C. § 103 as being unpatentable over Kinsley, Cordero, MacWilliams, Jeon, JEDEC1, and JEDEC2. Final Act. 12.

Claims 32, 37, and 42 stand rejected under 35 U.S.C. § 103 as being unpatentable over Kinsley, Cordero, MacWilliams, Jeon, JEDEC1, and JEDEC2. Final Act. 4.

Claims 7, 11, 19, and 27 stand rejected under 35 U.S.C. § 103 as being unpatentable over Kinsley, Cordero, MacWilliams, Jeon, and JEDEC2. Final Act. 17.

Claims 4, 12, 20, and 28 stand rejected under 35 U.S.C. § 103 as being unpatentable over Kinsley, Cordero, MacWilliams, Jeon, and Keller. Final Act. 18.

Claim 34 stands rejected under 35 U.S.C. § 103 as being unpatentable over Kinsley, Cordero, MacWilliams, Jeon, JEDEC1, and Keller. Final Act. 19.

Claims 5, 13, and 21 stand rejected under 35 U.S.C. § 103 as being unpatentable over Kinsley, Cordero, MacWilliams, Jeon, and JEDEC3. Final Act. 19-20.

[3] The statement of rejection in the Final Action does not mention Jeon. It is clear from the explanation of the rejection, however, that Jeon is meant to be included in the Examiner's combination of references. Final Act. 11–12.

Claims 35 and 39 stand rejected under 35 U.S.C. § 103 as being unpatentable over Kinsley, Cordero, MacWilliams, Jeon, JEDEC1, and JEDEC3. Final Act. 20.

Throughout this decision, we make reference to the Appeal Brief ("Appeal Br.," filed Jan. 17, 2019), the Reply Brief ("Reply Br.," filed Apr. 26, 2019), and the Examiner's Answer ("Ans.," mailed Feb. 26, 2019) for their respective details.

ISSUES

1. Does the specification provide written description support for the claim limitation "wherein as a condition to a change of the value to enable the PDA mode the DRAM device is to perform write leveling?"

2. Does the combination of Kinsley, Cordero, MacWilliams, and Jeon fairly suggest that, as a condition to a change of the value to enable the PDA mode, the DRAM device is to perform write leveling?

PRINCIPLES OF LAW

Under the written description requirement of 35 U.S.C. § 112, the disclosure of the application relied upon must reasonably convey to one of ordinary skill in the art that, as of the filing date of the application, the inventor had possession of the later-claimed subject matter. *Vas-Cath Inc. v. Mahurkar*, 935 F.2d 1555, 1563 (Fed. Cir. 1991). "One shows that one is 'in possession' of *the invention* by describing *the invention,* with all its claimed limitations, not that which makes it obvious." *Lockwood v. American Airlines, Inc.*, 107 F.3d 1565, 1572 (Fed. Cir. 1997) (emphasis in original).

ANALYSIS

35 U.S.C. § 112(a) rejection

Independent claims 1, 8, 16, 24, 31, 36, and 40 recite, in pertinent part, "wherein as a condition to a change of the value to enable the PDA mode the DRAM device is to perform write leveling," or analogous language.

The Examiner finds that this limitation is not described in the specification because "the specification only mentions that [before entering PDA mode,] 'a DRAM device may require write leveling.'" Final Act. 3; Spec. ¶ 16. The Examiner finds that "[a] skilled artisan would understand from Appellant's specification that certain embodiments may require write leveling before entering PDA mode, while other embodiments may not require write leveling before entering the PDA mode." Ans. 5.

We agree with the Examiner that the person of ordinary skill would understand Appellant's disclosure to be equivalent to the disclosure of two embodiments, one requiring write leveling, and one not requiring write leveling. We agree with Appellant that the specification "expressly teaches that write leveling may be required." Such disclosure, then, describes the invention, with all its claimed limitations, and conveys to one of ordinary skill in the art that the inventor had possession of the claimed subject matter. *Vas-Cath*, 935 F.2d at 1563; *Lockwood*, 107 F.3d at 1572.

We conclude that the Examiner erred in finding that the claimed invention lacks written description support. We do not sustain the Examiner's § 112 rejection of claims 1, 4-8, 10-14, 16, 18-22, 24, 26-29, 31, 32, 34-37, 39-42, 44-48, and 52-54.

35 U.S.C. § 103 rejection

Independent claim 1 recites a per-DRAM addressability (PDA) mode of a DRAM device, "wherein as a condition to a change of the value to enable the PDA mode the DRAM device is to perform write leveling." Independent claims 8, 16, 24, 31, 36, and 40 recite analogous limitations.

Jeon is relied upon to teach a write leveling operation. Jeon ¶ 112. Jeon teaches that write leveling can be initiated "when the memory system exits a deep power down mode of operation," "periodically," "when a change in impedance or temperature is detected," or "by the memory device itself." *Id*.

The Examiner reads the "change in impedance" option in Jeon on the claims under appeal. The Examiner finds that "[i]n PDA mode, the total impedance on the DQ pin is . . . dependent on the number of DRAM devices selected to be programmed, and thus, a write leveling operation must be initiated." Final Act. 7.

Appellant asserts that Kinsley (proposed to be modified in view of Jeon by the Examiner) teaches that the total impedance on the DQ0 line does not vary according to the number of DRAM devices selected to be programmed. Kinsley teaches "asserting EEFFFFFFFFFFFFFFFFh on DQ[71:0]," which asserts DQ[68] and DQ[64] logic low and asserts the rest of the lines logic high. Appeal Br. 14; Kinsley p. 10. Appellant argues that "all DRAM devices are connected to the DQ signal lines, otherwise they would not be able to 'listen' for an assertion of their DQ0." Appeal Br. 14. Appellant contends that if all DRAM devices are connected and monitoring the DQ signal line, all DRAM devices will be loading the signal line. *Id.*

Consequently, Appellant argues, PDA mode would not cause a change in impedance on the signal line. *Id.*

We agree with Appellant's argument. The Examiner responds in the Answer that

> [b]ecause PDA mode allows selected DRAM chips to be programmed, the net impedance on any one interconnect of a rank would change. In other words, if a rank has eighteen DRAM chips, and only two DRAM chips are selected for programming . . . the net impedance seen on any interconnect of the rank would change in PDA mode.

Ans. 10.

The Examiner finds that Kinsley teaches that line A4 must be set to logic '1' to place a DRAM in PDA mode. Ans. 13; Kinsley p. 8. "Therefore, Kinsley does not teach that all DRAM devices are connected and sampling or monitoring the DQ signal line." Ans. 13. The Examiner's finding does not contradict Appellant's argument that a DRAM device that is monitoring the DQ signal line is loading the signal line, thus causing no change in impedance.

Appellant further argues that Kinsley's process for turning off PDA mode supports its argument. Reply Br. 4-5; Kinsley p. 12. According to Kinsley, to exit PDA mode, all DRAM devices receive a logic '0' on DQ0. If the Examiner's interpretation were correct, only the two devices selected to be programmed in Kinsley's previous example would exit PDA mode, because the other seventy devices would be disconnected and unable to receive this command to exit PDA mode. Reply Br. 5.

We find, then, that Jeon does not teach that a DRAM device is to perform write leveling as a condition to a change of the value to enable the PDA mode, as the independent claims recite. We determine that the

Examiner's asserted combination of Kinsley, Cordero, MacWilliams, and Jeon does not teach or suggest all the limitations of the claimed invention. Accordingly, we do not sustain the Examiner's § 103 rejection of claims 1, 8, 14, 16, 22, 24, and 29 over Kinsley, Cordero, MacWilliams, and Jeon.

We do not sustain the Examiner's rejection of claims 31, 36, 40, 41, 44, and 52-54 over Kinsley, Cordero, MacWilliams, Jeon, and JEDEC1.

We do not sustain the Examiner's rejection of claims 6, 10, 18, and 26 over Kinsley, Cordero, MacWilliams, Jeon, and JEDEC1.

We do not sustain the Examiner's rejection of claims 45-48 over Kinsley, Cordero, MacWilliams, Jeon, JEDEC1, and JEDEC2.

We do not sustain the Examiner's rejection of claims 32, 37, and 42 over Kinsley, Cordero, MacWilliams, Jeon, JEDEC1, and JEDEC2.

We do not sustain the Examiner's rejection of claims 7, 11, 19, and 27 over Kinsley, Cordero, MacWilliams, Jeon, and JEDEC2.

We do not sustain the Examiner's rejection of claims 4, 12, 20, and 28 over Kinsley, Cordero, MacWilliams, Jeon, and Keller.

We do not sustain the Examiner's rejection of claim 34 over Kinsley, Cordero, MacWilliams, Jeon, JEDEC1, and Keller.

We do not sustain the Examiner's rejection of claims 5, 13, and 21 over Kinsley, Cordero, MacWilliams, Jeon, and JEDEC3.

We do not sustain the Examiner's rejection of claims 35 and 39 over Kinsley, Cordero, MacWilliams, Jeon, JEDEC1, and JEDEC3.

CONCLUSIONS

1. The specification provides written description support for the claim limitation "wherein as a condition to a change of the value to enable the PDA mode the DRAM device is to perform write leveling."

2. The combination of Kinsley, Cordero, MacWilliams, and Jeon does not teach or suggest that, as a condition to a change of the value to enable the PDA mode, the DRAM device is to perform write leveling.

DECISION SUMMARY

In summary:

Claims Rejected	35 U.S.C. §	Reference(s)/ Basis	Affirmed	Reversed
1, 4-8, 10-14, 16, 18-22, 24, 26-29, 31, 32, 34-37, 39-42, 44-48, 52-54	112	Written description		1, 4-8, 10-14, 16, 18-22, 24, 26-29, 31, 32, 34-37, 39-42, 44-48, 52-54
1, 8, 14, 16, 22, 24, 29	103	Kinsley, Cordero, MacWilliams, Jeon		1, 8, 14, 16, 22, 24, 29
31, 36, 40, 41, 44, 52-54	103	Kinsley, Cordero, MacWilliams, Jeon, JEDEC1		31, 36, 40, 41, 44, 52-54
6, 10, 18, 26	103	Kinsley, Cordero, MacWilliams, Jeon, and JEDEC1		6, 10, 18, 26
45-48	103	Kinsley, Cordero, MacWilliams, Jeon, JEDEC1, JEDEC2		45-48
32, 37, 42	103	Kinsley, Cordero, MacWilliams, Jeon, JEDEC1, JEDEC2		32, 37, 42
7, 11, 19, 27	103	Kinsley, Cordero, MacWilliams, Jeon, JEDEC2		7, 11, 19, 27
4, 12, 20, 28	103	Kinsley, Cordero, MacWilliams, Jeon, Keller		4, 12, 20, 28
34	103	Kinsley, Cordero, MacWilliams, Jeon, JEDEC1, Keller		34
5, 13, 21	103	Kinsley, Cordero, MacWilliams, Jeon, JEDEC3		5, 13, 21

Claims Rejected	35 U.S.C. §	Reference(s)/ Basis	Affirmed	Reversed
35, 39	103	Kinsley, Cordero, MacWilliams, Jeon, JEDEC1, JEDEC3		35, 39
Overall Outcome				1, 4-8, 10-14, 16, 18-22, 24, 26-29, 31, 32, 34-42, 44-48, 52-54

ORDER

The Examiner's decision to reject claims 1, 4-8, 10-14, 16, 18-22, 24, 26-29, 31, 32, 34-42, 44-48, and 52-54 is reversed.

REVERSED